This listing of claims replaces all prior versions, and listings of claims in the instant application:

Listing of Claims:

1. (Cancelled) Please Cancel Claim 1, without prejudice.

2. (Cancelled) Please Cancel Claim 2, without prejudice.

3. (Cancelled) Please Cancel Claim 3, without prejudice.

4. (Cancelled) Please Cancel Claim 4, without prejudice.

5. (Cancelled) Please Cancel Claim 5, without prejudice.

6. (Cancelled) Please Cancel Claim 6, without prejudice.

7. (Cancelled) Please Cancel Claim 7, without prejudice.

8. (Cancelled) Please Cancel Claim 8, without prejudice.

9. (Cancelled) Please Cancel Claim 9, without prejudice.

10. (Cancelled) Please Cancel Claim 10, without prejudice.

11. (Cancelled) Please Cancel Claim 11, without prejudice.

12. (Cancelled) Please Cancel Claim 12, without prejudice.

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13. (Cancelled) Please Cancel Claim 13, without prejudice.

14. (Cancelled) Please Cancel Claim 14, without prejudice.

15. (Cancelled) Please Cancel Claim 15, without prejudice.

16. (Cancelled) Please Cancel Claim 16, without prejudice.

17. (Cancelled) Please Cancel Claim 17, without prejudice.

18. (Cancelled) Please Cancel Claim 18, without prejudice.

19. (Cancelled) Please Cancel Claim 19, without prejudice.

20. (Cancelled) Please Cancel Claim 20, without prejudice.

21. (Cancelled) Please Cancel Claim 21, without prejudice.

22. (Cancelled) Please Cancel Claim 22, without prejudice.

23. (Cancelled) Please Cancel Claim 23, without prejudice.

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24. (Cancelled) Please Cancel Claim 24, without prejudice.

25. (Cancelled) Please Cancel Claim 25, without prejudice.

26. (Cancelled) Please Cancel Claim 26, without prejudice.

27. (Cancelled) Please Cancel Claim 27, without prejudice.

28. (Cancelled) Please Cancel Claim 28, without prejudice.

29. (Currently Amended) A method for maintaining translation lookaside buffer ("TLB") coherency in a computer system having a plurality of processors, each of the processors having an associated TLB for storing address translation data, the system having a main communication network coupled to the plurality of processors, said method comprising:

accessing a virtual address in a first TLB associated with one of the plurality of processors;

performing an operation on the first TLB based on the accessed virtual address and a physical address corresponding to the accessed virtual address;

generating a TLB message in response to a change in contents of the first TLB caused by the operation performed on the first TLB, the TLB message comprising an access request and at least one of the accessed virtual address and the corresponding physical address;

sending the TLB message to the plurality of processors other than the processor associated with the first TLB via the main communication network; and

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determining, at each of the plurality of processors other than that associated with the first TLB, if the TLB message affects the address translation data stored in the associated TLB in response to receiving the TLB message

~~The method in accordance with claim 1~~, wherein the operation causing a change in contents of the first TLB includes:

inputting a first entry into the first TLB when a physical address corresponding to the virtual address is not located in the first TLB;

moving a second entry from the first TLB to another location within the computer system, the second entry associated with a physical address corresponding to the virtual address; and

removing a third entry from the first TLB, the third entry associated with a physical address corresponding to the virtual address.

30. (Currently Amended) A method for maintaining translation lookaside buffer ("TLB") coherency in a computer system having a plurality of processors, each of the processors having an associated TLB for storing address translation data, the system having a main communication network coupled to the plurality of processors, said method comprising:

accessing a virtual address in a first TLB associated with one of the plurality of processors;

performing an operation on the first TLB based on the accessed virtual address and a physical address corresponding to the accessed virtual address;

generating a TLB message in response to a change in contents of the first TLB caused by the operation performed on the first TLB, the TLB message comprising an access request and at least one of the accessed virtual address and the corresponding physical address;

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sending the TLB message to the plurality of processors other than the processor associated with the first TLB via the main communication network; and

determining, at each of the plurality of processors other than that associated with the first TLB, if the TLB message affects the address translation data stored in the associated TLB in response to receiving the TLB message, wherein the TLB message comprises:

a request for a read access to a first entry to add the address translation data into the associated TLB in each of the plurality of processors, further

~~The method in accordance with claim 2,~~ wherein the TLB message comprises both of the accessed virtual address and the corresponding physical address.

31. (Currently Amended) A method for maintaining translation lookaside buffer ("TLB") coherency in a computer system having a plurality of processors, each of the processors having an associated TLB for storing address translation data, the system having a main communication network coupled to the plurality of processors, said method comprising:

accessing a virtual address in a first TLB associated with one of the plurality of processors;

performing an operation on the first TLB based on the accessed virtual address and a physical address corresponding to the accessed virtual address;

generating a TLB message in response to a change in contents of the first TLB caused by the operation performed on the first TLB, the TLB message comprising an access request and at least one of the accessed virtual address and the corresponding physical address;

sending the TLB message to the plurality of processors other than the processor associated with the first TLB via the main communication network; and

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determining, at each of the plurality of processors other than that associated with the first TLB, if the TLB message affects the address translation data stored in the associated TLB in response to receiving the TLB message, wherein the TLB message comprises:

a request for a write access to a second entry to modify all copies of the second entry in the associated TLB of each of the plurality of processors, further

~~The method in accordance with claim 3,~~ wherein the TLB message comprises both of the accessed virtual address and the corresponding physical address.

32. (Cancelled) Please cancel Claim 32, without prejudice.

33. (Currently Amended) An apparatus for maintaining translation lookaside buffer ("TLB") coherency in a computer system including a plurality of processors, each of the plurality of processors having an associated TLB for storing address translation data, said apparatus comprising:

means for accessing a virtual address in a first TLB associated with one of the plurality of processors;

means for performing an operation on the first TLB based on the accessed virtual address and a physical address corresponding to the accessed virtual address;

means for generating a TLB message in response to a change in contents of the first TLB caused by the operation performed on the first TLB, the TLB message comprising an access request and at least one of the accessed virtual address and the corresponding physical address;

means for sending the TLB message to the plurality of processors other than the processor associated with the first TLB via the main communication network; and

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means for determining, at each of the plurality of processors other than that associated with the first TLB, if the TLB message affects the address translation data stored in the associated TLB in response to receiving the TLB message

~~The apparatus in accordance with claim 20~~, wherein the operation causing a change in contents of the first TLB includes:

inputting a first entry into the first TLB when a physical address corresponding to the virtual address is not located in the first TLB;

moving a second entry from the first TLB to another location within the computer system, the second entry associated with a physical address corresponding to the virtual address; and

removing a third entry from the first TLB, the third entry associated with a physical address corresponding to the virtual address.

34. (Currently Amended) An apparatus for maintaining translation lookaside buffer ("TLB") coherency in a computer system including a plurality of processors, each of the plurality of processors having an associated TLB for storing address translation data, said apparatus comprising:

means for accessing a virtual address in a first TLB associated with one of the plurality of processors;

means for performing an operation on the first TLB based on the accessed virtual address and a physical address corresponding to the accessed virtual address;

means for generating a TLB message in response to a change in contents of the first TLB caused by the operation performed on the first TLB, the TLB message comprising an access request and at least one of the accessed virtual address and the corresponding physical address;

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means for sending the TLB message to the plurality of processors other than the processor associated with the first TLB via the main communication network; and

means for determining, at each of the plurality of processors other than that associated with the first TLB, if the TLB message affects the address translation data stored in the associated TLB in response to receiving the TLB message, wherein

said means for transmitting comprises:

means for interconnecting each of the plurality of a processors to one another via corresponding one of the plurality of independent paths, further

~~The apparatus in accordance with claim 21,~~ wherein the TLB message comprises both of the accessed virtual address and the corresponding physical address.

35. (Currently Amended) An apparatus for maintaining translation lookaside buffer ("TLB") coherency in a computer system including a plurality of processors, each of the plurality of processors having an associated TLB for storing address translation data, said apparatus comprising:

means for accessing a virtual address in a first TLB associated with one of the plurality of processors;

means for performing an operation on the first TLB based on the accessed virtual address and a physical address corresponding to the accessed virtual address;

means for generating a TLB message in response to a change in contents of the first TLB caused by the operation performed on the first TLB, the TLB message comprising an access request and at least one of the accessed virtual address and the corresponding physical address;

means for sending the TLB message to the plurality of processors other than the processor associated with the first TLB via the main communication network; and

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means for determining, at each of the plurality of processors other than that associated with the first TLB, if the TLB message affects the address translation data stored in the associated TLB in response to receiving the TLB message, wherein the TLB message comprises:

a request for a read access to a first entry to add the address translation data into the associated TLB in each of the plurality of processors, further

~~The apparatus in accordance with claim 22,~~ wherein the TLB message comprises both of the accessed virtual address and the corresponding physical address.

36. (Cancelled) Please cancel Claim 36, without prejudice.

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